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(54) A thin-film transistor array

Dünnfilm-Transistormatrix

Matrice de transistors à couche mince

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(73) Proprietor: **SHARP KABUSHIKI KAISHA**
Osaka 545 (JP)

(72) Inventors:
- **Hishida, Tadanori**
  Kashihara-shi Nara-ken (JP)
- **Shoji, Hajime**
  Higashiosaka-shi Osaka (JP)
- **Hamada, Hiroshi**
  Nara-shi Nara-ken (JP)
- **Nagatomi, Hisato**
  Tenri-shi Nara-ken (JP)

(74) Representative: **Huntingford, David Ian et al**
W.P. THOMPSON & CO.
Coopers Building
Church Street
Liverpool L1 3AB (GB)

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- **PATENT ABSTRACTS OF JAPAN vol. 10, no. 129 (E-403)(2186) 14 May 1986 & JP-A- 60 261 174 (NIPPON JIDOSHA BUHIN SOGO KENKYUSHO) 24 December 1985**
- **PATENT ABSTRACTS OF JAPAN vol. 1, no. 91 (E-394)9 April 1986 & JP-A- 60 233 860 (NIPPON JIDOSHA BUHIN SOGO KENKYUSHO) 20 November 1985**

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Description

This invention relates to an improvement in thin-film transistor arrays that are used in, for example, colored liquid-crystal display devices, and more particularly, to thin-film silicon transistor arrays with a thin-film structure improved at the intersections of the gate bus lines and the source bus lines.

As a typical example of conventional thin-film transistor arrays, Figure 4 shows a thin-film silicon transistor array that is used in a liquid-crystal display panel. In this example, a number of thin-film transistors 1 are arranged in a matrix form to construct a liquid-crystal display device of the active-matrix type. Each thin-film transistor 1 is driven by the input of a scanning signal from the gate bus line 2. With the input of a picture signal from the source bus line 3, the liquid-crystal display panel is operated by the thin-film transistor 1 via the picture-element electrode 4.

In conventional thin-film transistor arrays of this type, intersections X1 of the gate bus lines 2 and the source bus lines 3 have the structure shown in Figures 5 to 7. That is, on the top of an insulating substrate 5 made of a glass or the like, there is formed the gate bus line 2 made of tantalum (Ta) with a thickness of 100 to 400nm (1000 to 4000 Å). On the surface of the gate bus line 2, an insulating film 6 made of tantalum oxide (Ta_2O_5) is formed by anodic oxidation. Then, by plasma chemical vapor deposition, a layered structure is formed which comprises successively a gate insulating film 7 made of SiN_x with a thickness of 100 to 300nm (1000 to 3000 Å), an amorphous silicon (a-Si) film 8 with a thickness of 10 to 20nm (100 to 200 Å), and a protective insulating film 9 made of SiN_x with a thickness of 100 to 400nm (1000 to 4000 Å). After the deposition of protective insulating film 9, patterning thereof is done by etching. Thereafter, a phosphorous-doped n^+-type a-Si film 10 with a thickness of 10 to 100nm (100 to 1000 Å) is deposited thereon, and a patterning of both the n^+ type a-Si film 10 and the a-Si film 8 at the same time gives the configuration shown in Figures 6 and 7. Moreover, the width of the SiN_x protective insulating film 9 is less than that of the n^+-type a-Si film 10 and of the a-Si film 8 in both directions in which the gate bus line extends.

The source bus line 3 and the drain bus line 11 (shown in Figure 5) are formed on the layered structure mentioned above by the pattering of deposited Ti. The picture-element electrodes 4 are formed by the patterning of a transparent conductive film such as indium-tin-oxide (ITO) after the deposition.

With a liquid-crystal display device using the thin-film silicon transistor array mentioned above, cross talk between the picture elements can be reduced, resulting in a display with a large capacity and high picture quality.

At the present, various devices using a thin-film transistor array such as liquid-crystal display devices and the like are extremely expensive because of the complexity of the panel construction. The structure of the thin-film transistor array itself is as described above, so that it is difficult to reduce the production cost. Thus, the use of a more inexpensive driver to be connected may be considered as one way to reduce the cost of devices using a thin-film transistor array such as liquid-crystal display devices and the like.

However, in the intersection X1 of the source bus line 3 and the gate bus line 2 mentioned above for the conventional thin-film transistor arrays, the electric capacity is formed by the gate bus line 2, the insulating films 6, the gate insulating film 7, and the a-Si film 8; because this electric capacity is relatively large, the drive load becomes large. Therefore, it is necessary to connect a source driver and gate driver with large driving capacity, which makes it difficult to use inexpensive drivers.

There is known from DE-A- 3 640 174 a thin-film transistor array comprising an insulating substrate; a plurality of thin-film transistors disposed in a matrix form on said substrate; a plurality of gate bus lines formed parallel to each other on said substrate, each of said gate bus lines being connected electrically with the gate electrodes of the thin-film transistors in the corresponding row of said matrix; and a plurality of source bus lines formed perpendicular to said gate bus lines on said substrate, each of said source bus lines being connected electrically with the source electrodes of the thin-film transistors in the corresponding column of said matrix. At the intersections of said gate bus lines and said source bus lines, there is disposed a layered structure between the gate bus lines and the source bus line, comprising successively a gate insulating film, a first semiconductor film, a protective insulating film, and a second semiconductor film which is connected electrically with said source bus line. In the latter arrangement of D1, the second semi-conductor film extends continuously over the source bus lines and the thin film transistors.

It is an object of the present invention to provide a thin-film transistor array which overcomes the above-discussed and other disadvantages and deficiencies of the known arrangements.

In accordance with the invention there is provided a thin-film transistor array which comprises an insulating substrate; a plurality of thin-film transistors disposed in a matrix form on said substrate; a plurality of gate bus lines formed parallel to each other on said substrate each of said gate bus lines being connected electrically with the gate electrodes of the thin-film transistors in the corresponding row of said matrix; and a plurality of source bus lines formed perpendicular to said gate bus lines on said substrate, each of said source bus lines being connected electrically with the source electrodes of the thin-film transistors in the corresponding column of said matrix; wherein at the intersections of said gate bus lines and said source bus lines, there is disposed a layered structure between the gate bus line and the source bus line, comprising successively a gate insulat-

ing film, a first semiconductor film, a protective insulating film, and a second semiconductor film that is connected electrically with said source bus line; and wherein at said intersections, the width of said protective insulating film in the direction in which said gate bus line extends is equal to or greater than that of said second semiconductor film in said direction to separate said second semiconductor film electrically from said first semiconductor film, and the first semi-conductor film, the protective insulating film and the second semi-conductor film are laterally separated from the thin film transistors.

In a preferred embodiment, the insulating substrate is made of a glass.

In a preferred embodiment, the insulating substrate in the gate bus lines are made of tantalum and said source bus lines are made of titanium.

In a more preferred embodiment, an insulating film made of tantalum oxide is disposed on the surface of said gate bus lines.

In a preferred embodiment, the gate insulating film comprises an SiN_x gate insulating film with a thickness of 100 to 300nm (1000 to 3000 Å), said first semiconductor film comprises an amorphous silicon film with a thickness of 10 to 20nm (100 to 200 Å), said protective insulating film comprises SiN_x protective insulating film with a thickness of 100 to 400nm (1000 to 4000 Å), and said second semiconductor film comprises a phosphorous-doped n^+-type amorphous silicon film with a thickness of 10 to 100nm (100 to 1000 Å).

In a preferred embodiment, the gate insulating film, said first semiconductor film, said protective insulating film, and said second semiconductor film are formed by plasma chemical vapor deposition.

Thus, the invention described herein makes possible the provision of (1) a thin-film transistor array in which the protective insulating film separates the second semiconductor film formed above it electrically from the first semiconductor film formed below it, so that the electric capacity of the protective insulating film contributes to the electric capacity of the intersections of the source bus line and the gate bus line, thereby making it possible to decrease the electric capacity of the said intersections effectively; (2) a thin-film transistor array that has a lowered driving load, so that the drivers to be connected therewith require a lesser driving capacity, thereby making it possible to drive the display devices with more inexpensive drivers; (3) a thin-film transistor array by which the chips used in the drivers can be made smaller, so that the number of chips formed from a mother wafer increases, thereby making it possible to decrease the cost of the drivers; and (4) a thin-film transistor array that can make extremely large contributions to a decrease in the cost of the display devices such as colored liquid-crystal televisions.

The invention is described further hereinafter, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is an enlarged top plan view showing a portion of a thin-film transistor array of this invention;

Figure 2 is an enlarged cross-sectional view taken along line II-II of Figure 1;

Figure 3 is an enlarged cross-sectional view taken along line III-III of Figure 1;

Figure 4 is a schematic top plan view showing a liquid-crystal display device using a thin-film transistor array;

Figure 5 is an enlarged top plan view showing a portion of a conventional thin-film transistor array;

Figure 6 is an enlarged cross-sectional view taken along line VI-VI of Figure 5;

Figure 7 is an enlarged cross-sectional view taken along line VII-VII of Figure 5;

Figures 8 and 9 are enlarged cross-sectional views for illustrating the operation of the conventional thin-film transistor array; and

Figures 10 and 11 are enlarged cross-sectional views for illustrating the operation of the thin-film transistor array of Figure 1.

In the thin-film transistor array of this invention, the first semiconductor film formed above the gate bus line is regarded as a conductor, because electric charge is accumulated therein when the gate bus line is turned on. The protective insulating film formed on the first semiconductor film is wider than the second semiconductor film formed on the protective insulating film, or else is of the same width. Therefore, there is complete electrical separation between the first semiconductor film and the second semiconductor film in the said direction.

In this way, because there is complete electrical separation between the first semiconductor film and the second semiconductor film, the electric capacity is also formed by the first semiconductor film, the protective insulating film, and the second semiconductor film. This electric capacity is connected in series with the capacity that is formed by the gate bus line, the gate insulating film, and the first semiconductor film. For this reason, the total electric capacity of the intersections is decreased, so that the driving load of the thin-film transistor array can be decreased.

Examples

Figure 1 is an enlarged top plan view showing a portion of the thin-film silicon transistor array of this invention. Figures 2 and 3 are enlarged cross-sectional views

taken along line II-II and line III-III respectively, of Figure 1.

In Figure 1, the example of this invention to be described below is illustrated at the intersection X2 of the gate bus line 22 and the source bus line 23. Moreover, in Figure 1, reference numeral 21 is a thin-film transistor, and reference numeral 24 is a picture-element electrode. The manufacturing process of the thin-film silicon transistor array will hereinafter be described, of this example which makes clear the layered structure at the intersection X2.

First, on the top of an insulating substrate 25 made of a glass or the like, there is formed the gate bus line 22 made of tantalum (Ta) with a thickness of 1000 to 400nm (1000 to 4000 Å) and on the surface of the gate bus line 22, insulating film 26 made of tantalum oxide (Ta_2O_5) is formed by anodic oxidation. Then, by plasma chemical vapor deposition, a layered structure is formed which comprises successively a gate insulating film 27 made of SiN_x with a thickness of 100 to 300nm (1000 to 3000 Å), an amorphous silicon (a-Si) film 28 with a thickness of 10 to 20nm (100 to 200 Å), and a protective insulating film 29 made of SiN_x with a thickness of 100 to 400nm (1000 to 4000 Å). Next, patterning of this SiN_x protective insulating film 29 is done by etching.

Thereafter, phosphorus-doped n^+-type a-Si film 30 with a thickness of 10 to 100nm (100 to 1000 Å) is deposited thereon, and this n^+-type a-Si film 30 and the a-Si film 28 are patterned at the same time. At this-time, the width of the n^+-type a-Si film 30 is made less than that of the SiN_x protective insulating film 29 at both sides in the direction in which the gate bus line 22 extends, as shown in Figure 3.

Then, the source bus line 23 and the drain bus line 31 are formed by the patterning of deposited Ti, which is the metal used for the source and the drain bus lines. Moreover, a transparent conductive film made of indium-tin-oxide (ITO) is deposited and patterned to form the picture elements 24.

The operation of this example will hereinafter be explained by reference to Figures 8 to 11 in comparison with the conventional example given above. In Figures 8 to 11, only the portions that are regarded as a conductor are hatched.

(1) Electric capacity of the intersection X1 in the conventional example

Figures 8 and 9 are enlarged cross-sectional views showing the same conventional example as in Figures 6 and 7. In the conventional example, when the gate bus line 2 is turned on, there is accumulation of electric charge in the a-Si film 8 formed above the gate bus line 2. Therefore, as is shown by the hatching in Figures 8 and 9, the a-Si film 8 can be regarded as a conductor. The SiN_x protective insulating film 9 is enclosed with the conductors (i.e., the portions shown by the slanted hatching in Figures 8 and 9), so that the electric capacity of the intersection X1 is not affected by the protective insulating film 9. Thus, the electric capacity of the intersection X1 can be considered to be formed by the Ta_2O_5 insulating film 6 and the SiN_x protective insulating film 7 only. Therefore, when the electric capacity of the Ta_2O_5 insulating film 6 is Ca, and the electric capacity of the SiN_x protective insulating film 7 is Cb, the total electric capacity C_1 of the intersection X1 is given by the expression:

$$(1/C_1) = (1/Ca) + (1/Cb)$$

(2) Electric capacity of the intersection X2 in the example of this invention

Next, the electric capacity of the intersection X2 in the example given above will be considered by reference to Figures 10 and 11. When the gate bus line 22 is turned on, as described above, there will be accumulation of electric charge in the a-Si film 28 formed above the gate bus line 22; the portions with hatching in these figures can be regarded as a conductor. In this example, as can be seen from Figure 11, the SiN_x protective insulating film 29 completely separates the a-Si film 28 and the n^+-type a-Si film 30 from each other. Thus, the electric capacity of the intersection X2 is affected by the electric capacity of this SiN_x protective insulating film 29. Therefore, when the electric capacity based on the SiN_x protective insulating film 29 is Cx, the total electric capacity C_2 of the intersection X2 is given by the expression:

$$(1/C_2) = (1/Ca) + (1/Cb) + (1/Cx)$$

As is clear from the expressions to calculate C_1 and C_2, the inequality $C_2 < C_1$ nodes. Therefore, according to the example of this invention, the electric capacity of the intersections of the source bus lines and the gate bus lines can be effectively decreased in comparison with the electric capacity in the conventional example.

Claims

1. A thin-film transistor array comprising

an insulating substrate (25);
a plurality of thin-film transistors (21) disposed in a matrix form on said substrate;
a plurality of gate bus lines (22) formed parallel to each other on said substrate (25), each of said gate bus lines (22) being connected electrically with the gate electrodes of the thin-film transistors (21) in the corresponding row of said matrix; and
a plurality of source bus lines (23) formed per-

pendicular to said gate bus lines (22) on said substrate, each of said source bus lines (23) being connected electrically with the source electrodes of the thin-film transistors in the corresponding column of said matrix;
wherein at the intersections of said gate bus lines (22) and said source bus lines (23), there is disposed a layered structure between the gate bus line and the source bus line, comprising successively a gate insulating film (27), a first semiconductor film (28), a protective insulating film (29), and a second semiconductor film (30) which is connected electrically with said source bus line (23);

characterised in that, at said intersections, the width of said protective insulating film (29) in the direction in which said gate bus line (22) extends is equal to or greater than that of said second semiconductor film (30) in said direction to separate said second semiconductor film (30) electrically from said first semiconductor film (28), and the first semiconductor film (28), the protective insulating film (29) and the second semi-conductor film (30) are laterally separated from the thin film transistors (21).

2. A thin-film transistor array according to claim 1, wherein said insulating substrate (25) is made of a glass.

3. A thin-film transistor array according to claim 1, wherein said gate bus lines (22) are made of tantalum and said source bus lines (23) are made of titanium.

4. A thin-film transistor array according to claim 3, wherein an insulating film (26) made of tantalum oxide is disposed on the surface of said gate bus lines (22).

5. A thin-film transistor array according to claim 1, wherein said gate insulating film (27) comprises an SiN_x gate insulating film with a thickness of 100 to 300nm (1000 to 3000 Å), said first semiconductor film (28) comprises an amorphous silicon film with a thickness of 10 to 20nm (100 to 200 Å), said protective insulating film (29) comprises an SiN_x protective insulating film with a thickness of 100 to 400nm (1000 to 4000 Å), and said second semiconductor film (30) comprises a phosphorous-doped n^+-type amorphous silicon film with a thickness of 10 to 100nm (100 to 1000 Å).

Patentansprüche

1. Dünnfilm-Transistormatrix mit:

- einem isolierenden Substrat (25);
- einer Vielzahl von Dünnfilmtransistoren (21), die in Matrixform auf dem Substrat angeordnet sind;
- einer Vielzahl von Gatebusleitungen (22), die parallel zueinander auf dem Substrat (25) ausgebildet sind und jeweils elektrisch mit den Gateelektroden der Dünnfilmtransistoren (21) in der entsprechenden Zeile der Matrix verbunden sind; und
- einer Vielzahl von Sourcebusleitungen (23), die rechtwinklig zu den Gatebusleitungen (22) auf dem Substrat ausgebildet sind und jeweils elektrisch mit den Sourceelektroden der Dünnfilmtransistoren in der entsprechenden Spalte der Matrix verbunden sind;
- wobei an den Schnittstellen der Gatebusleitungen (22) mit den Sourcebusleitungen (23) eine Schichtstruktur zwischen der Gatebusleitung und der Sourcebusleitung angeordnet ist, die aufeinanderfolgend aus einem Gateisolierfilm (27), einem ersten Halbleiterfilm (28), einem Schutzisolierfilm (29) und einem zweiten Halbleiterfilm (30), der elektrisch mit der Sourcebusleitung (23) verbunden ist, besteht;

dadurch gekennzeichnet, dass die Breite des Schutzisolierfilms (29) in der Richtung, in der sich die Gatebusleitung (22) erstreckt, gleich groß oder größer ist als die des zweiten Halbleiterfilms (30) in dieser Richtung, um den zweiten Halbleiterfilm (30) elektrisch vom ersten Halbleiterfilm (28) zu trennen, und der erste Halbleiterfilm (28), der Schutzisolierfilm (29) und der zweite Halbleiterfilm (30) lateral von den Dünnfilmtransistoren (21) getrennt sind.

2. Dünnfilm-Transistormatrix nach Anspruch 1, bei der das isolierende Substrat (25) aus Glas besteht.

3. Dünnfilm-Transistormatrix nach Anspruch 1, bei der die Gatebusleitungen (22) aus Tantal und die Sourcebusleitungen (23) aus Titan bestehen.

4. Dünnfilm-Transistormatrix nach Anspruch 3, bei der der aus Tantaloxid bestehende Isolierfilm (26) auf der Oberfläche der Gatebusleitungen (22) angeordnet ist.

5. Dünnfilm-Transistormatrix nach Anspruch 1, bei der der Gateisolierfilm (27) ein SiN_x-Gateisolierfilm mit einer Dicke von 100 bis 300 nm (1000 bis 3000 Å) ist, der erste Halbleiterfilm (28) ein Film aus amorphem Silicium mit einer Dicke von 10 bis 20 nm (100 bis 200 Å) ist, der Schutzisolierfilm (29) ein SiN_x-Schutzisolierfilm mit einer Dicke von 100 bis 400 nm (1000 bis 4000 Å) ist und der zweite Halbleiterfilm (30) ein mit Phosphor dotierter Film aus amorphem Silicium vom n^+-Typ mit einer Dicke von 10 bis 100

nm (100 bis 1000 Å) ist.

Revendications

1. Matrice de transistors à couches minces comprenant :

   un substrat isolant (25) ;
   une pluralité de transistors à couches minces (21) disposés sous forme de matrice sur ledit substrat ;
   une pluralité de lignes de bus de grille (22) formées parallèlement les unes aux autres sur ledit substrat (25), chacune desdites lignes de bus de grille (22) étant raccordée électriquement aux électrodes de grille des transistors à couches minces (21) dans la rangée correspondante de ladite matrice ; et
   une pluralité de lignes de bus de source (23) formées perpendiculairement aux dites lignes de bus de grille (22) sur ledit substrat, chacune desdites lignes de bus de source (23) étant connectée électriquement aux électrodes de source des transistors à couches minces dans la colonne correspondante de ladite matrice ;
   dans laquelle aux intersections desdites lignes de bus de grille (22) et desdites lignes de bus de source (23), est disposée une structure stratifiée entre la ligne de bus de grille et la ligne de bus de source, comprenant successivement un film d'isolation de grille (27), un premier film semi-conducteur (28), un film isolant de protection (29) et un second film semi-conducteur (30) connecté électriquement à ladite ligne de bus de source (23) ;

   caractérisé en ce que, aux dites intersections, la largeur dudit film isolant de protection (29) dans la direction duquel ladite ligne de bus de grille (22) se prolonge est égale ou supérieure à celle dudit second film semi-conducteur (30) dans ladite direction afin de séparer ledit second film semi-conducteur (30) électriquement dudit premier film semi-conducteur (28), et le premier film semi-conducteur (28), le film isolant de protection (29) et le second film semi-conducteur (30) sont séparés latéralement des transistors à couches minces (21).

2. Matrice de transistors à couches minces selon la revendication 1, dans laquelle ledit substrat isolant (25) est constitué de verre.

3. Matrice de transistors à couches minces selon la revendication 1, dans laquelle lesdites lignes de bus de grille (22) sont constituées de tantale et lesdites lignes de bus de source (23) sont constituées de titane.

4. Matrice de transistors à couches minces selon la revendication 3, dans laquelle un film d'isolation (26) constitué d'oxyde de tantale est disposé à la surface desdites lignes de bus de grille (22).

5. Matrice de transistors à couches minces selon la revendication 1, dans laquelle ledit film d'isolation de grille (27) comprend un film d'isolation de grille en SiN_x d'une épaisseur de 100 à 300 nm (1000 à 3000 Å), ledit premier film semi-conducteur (28) comporte un film de silicium amorphe d'une épaisseur de 10 à 20 nm (100 à 200 Å), ledit film isolant de protection (29) comprend un film isolant de protection en SiN_x d'une épaisseur de 100 à 400 nm (1000 à 4000 Å), et ledit second film semi-conducteur (30) comporte un film de silicium amorphe de type n^+ dopé au phosphore d'une épaisseur de 10 à 100 nm (100 à 1000 Å).

Fig 1

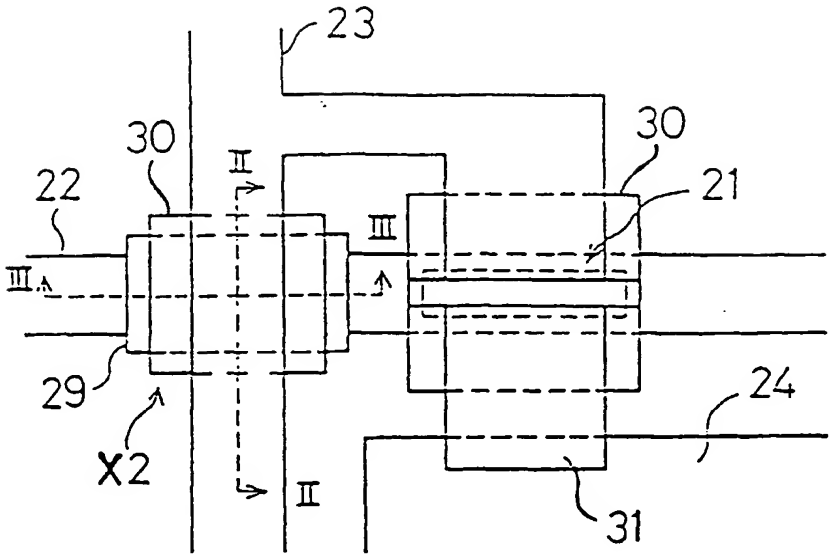

Fig 2

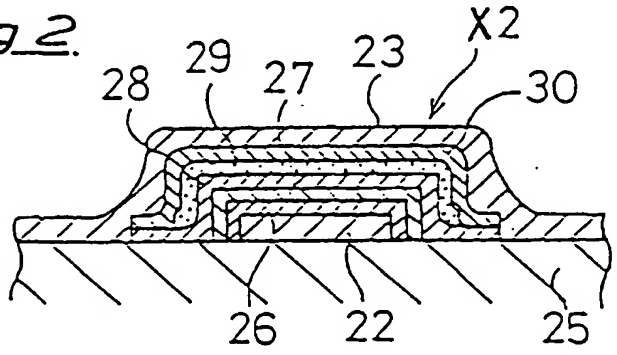

Fig 3

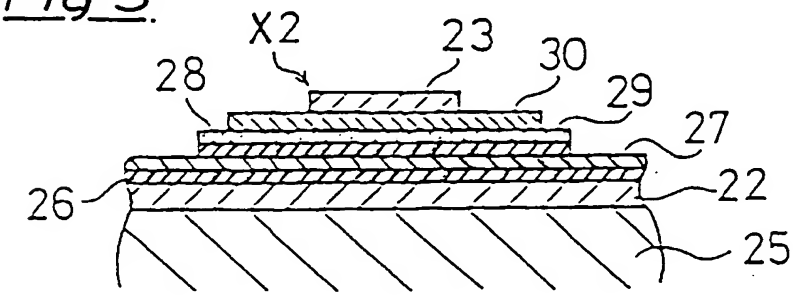

Fig 4 PRIOR ART

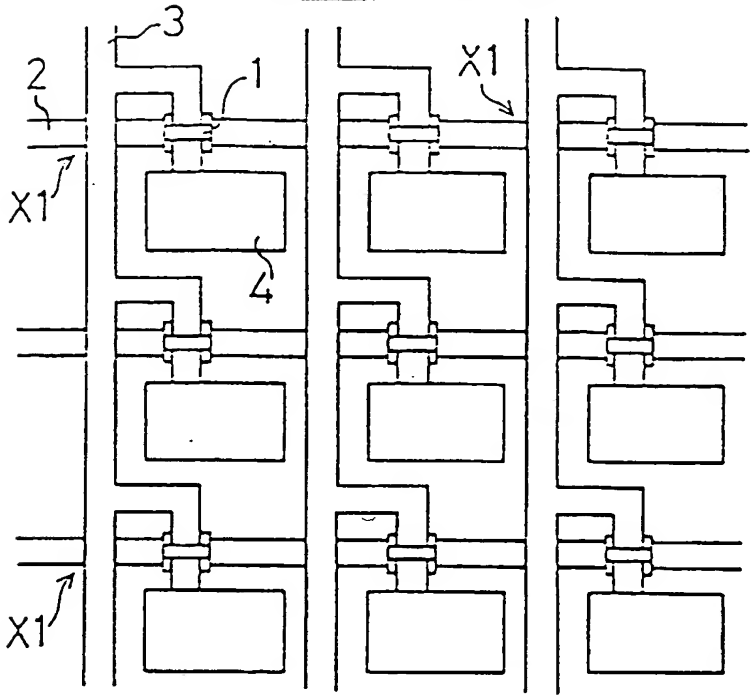

Fig 5 PRIOR ART

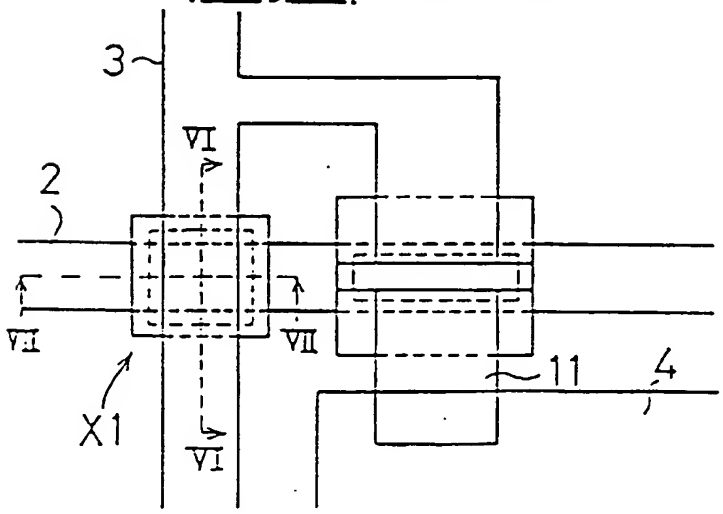

Fig 6. PRIOR ART

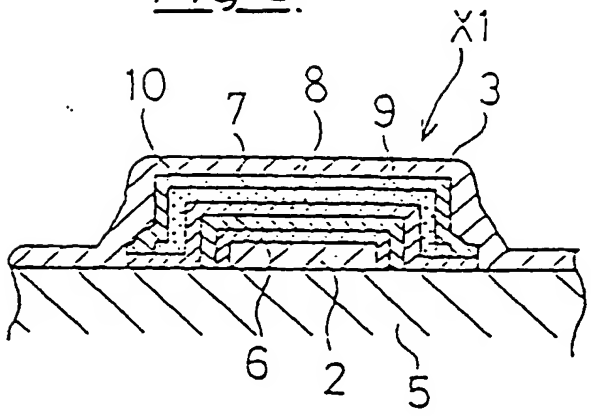

Fig 7. PRIOR ART

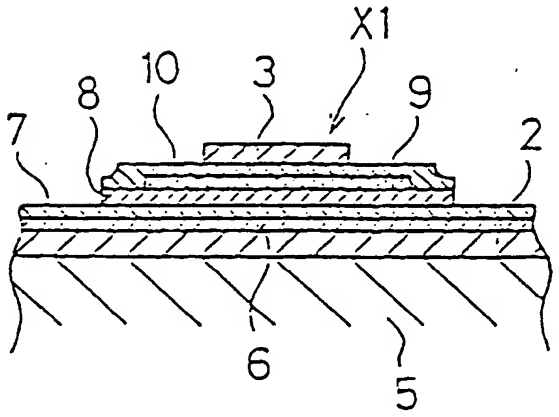

Fig 8 PRIOR ART

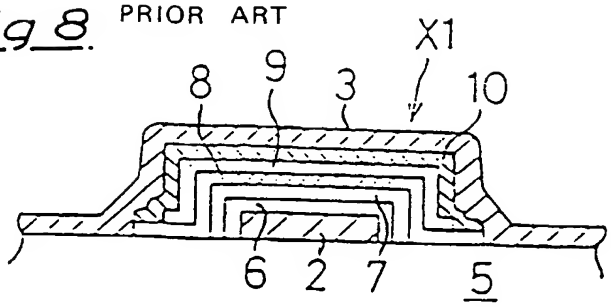

Fig 9 PRIOR ART

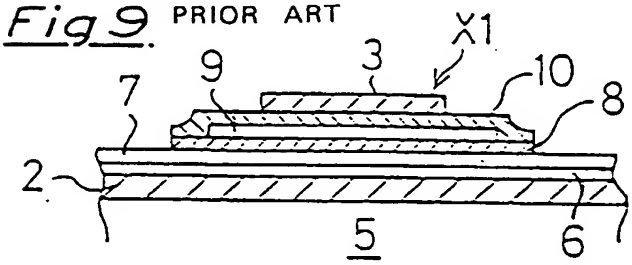

Fig 10

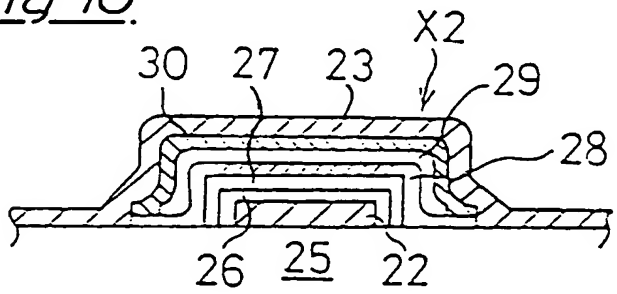

Fig 11